**EAST WEST UNIVERSITY**

**Department of Computer Science and Engineering  
  
Semester:** Spring 2017  
**Course Number:** CSE345  
**Course Title:** Digital Logic Design

**Experiment Number:** 02  
**Experiment Title:** Design and Implementation of a Combination Circuits

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**Objectives:**

* To design a combinational circuit from descriptive problem specification.
* To implement a combinational circuit using AND-OR and OR-AND logic.

**Answers to the Post-Lab Questions**

**1. Truth Table**

**Sum of Products:** F (A, B, C, D) = A + BC

|  |  |
| --- | --- |
| **A B C D** | **F** |
| 0 0 0 0 | 0 |
| 0 0 0 1 | 0 |
| 0 0 1 0 | 0 |
| 0 0 1 1 | 0 |
| 0 1 0 0 | 0 |
| 0 1 0 1 | 0 |
| 0 1 1 0 | 1 |
| 0 1 1 1 | 1 |
| 1 0 0 0 | 1 |
| 1 0 0 1 | 1 |
| 1 0 1 0 | 1 |
| 1 0 1 1 | 1 |
| 1 1 0 0 | 1 |
| 1 1 0 1 | 1 |
| 1 1 1 0 | 1 |
| 1 1 1 1 | 1 |

**Product of Sums:** F (A, B, C, D) = (A + B)(A + C)

|  |  |
| --- | --- |
| **A B C D** | **F** |
| 0 0 0 0 | 0 |
| 0 0 0 1 | 0 |
| 0 0 1 0 | 0 |
| 0 0 1 1 | 0 |
| 0 1 0 0 | 0 |
| 0 1 0 1 | 0 |
| 0 1 1 0 | 1 |
| 0 1 1 1 | 1 |
| 1 0 0 0 | 1 |
| 1 0 0 1 | 1 |
| 1 0 1 0 | 1 |
| 1 0 1 1 | 1 |
| 1 1 0 0 | 1 |
| 1 1 0 1 | 1 |
| 1 1 1 0 | 1 |
| 1 1 1 1 | 1 |

**2. Structural Verilog Code**

**Sum of Products:** F (A, B, C, D) = A + BCmodule exp2\_1( input A,B,C ,   
 output F);  
 wire w1,w2;   
 and g1 (w1, A),  
 g2 (w2 ,B,C),  
 or g3( F, w1, w2 );  
endmodule

**Product of Sums:** F (A, B, C, D) = (A + B)(A + C)

module exp2\_2 (input A, B, C,   
 output F);  
 wire w1, w2, w3;  
 or g1( A,B),  
 g2 (A,C),  
 and g3( F, w1, w2);  
endmodule

**Conclusion:**

In this experiment, getting the output of a combinational circuit we have used pin diagram of the required ICs. By using AND gates and OR gates, we verified the truth table from the circuit.